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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,306	11/04/2003	Hea Suk Jung	CU-3424 VE	5038
26530	7590	12/21/2004	EXAMINER	
LADAS & PARRY LLP			NGUYEN, LINH M	
224 SOUTH MICHIGAN AVENUE			ART UNIT	PAPER NUMBER
SUITE 1200				2816
CHICAGO, IL 60604				

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/701,306	JUNG, HEA SUK	
	Examiner Linh M. Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 04 November 2003.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-7 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-7 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 04 November 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/17/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

Claims 1-7 are presented in the instant application according to the Applicant's filing on 11/04/2003.

### *Abstract*

1. The abstract of the disclosure is objected to because it contains more than 150 words.
2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Appropriate correction is required.

### *Claim Objections/Minor Informalities*

3. Claims 3, 6 and 7 are objected to because of the following informalities:

Claim 3, lines 1 and 4, it is suggested to change "if" to -- when-- to recite unconditional limitations.

Claim 6, it is suggested to change "6" to --1-- since claim 6 cannot depend on itself.

Claim 7, it is suggested to either (a) change "steps" to --step-- or (b) add more steps to the claim.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

Art Unit: 2816

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 7, lines 7-8, the recitation “respectively dividing a frequency of the input clock signal into 1/2” appears to be indefinite since it is unclear which input is being referred to; is it the external input clock (line 3) or the internal input clock (line 3).

Clarification is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. , “A Low-Noise CMOS Prescaler for 900 MHz to 1.9 GHz Wireless Applications”, IEEE 1999 Custom Integrated Circuits Conference, pp. 597-600.

With respect to claim 1, Chang et al. discloses, in Fig. 1, clock divider for a DLL (Delay Lock Loop) circuit of a synchronous memory device for synchronization an external input clock with an internal input clock, the clock divider comprising a) M (where M is an integer that is larger than 2) [x8, x9, x10, x11] dividers connected in series; and b) power-down controller [X12] for receiving an output signal of the (M-1)-th divider [x10] and an output signal of the

M-th divider [x11], and selectively outputting the output signals; wherein the respective dividers divide a frequency of a clock signal inputted to the respective dividers into 1/2.

With respect to claim 2, Chang et al. discloses, in Fig. 1, that the output signal of the power-down controller has frequency obtained by dividing the frequency of the clock signal divider into  $1/2^M$  or  $1/2^{(M-1)}$  in accordance with a logic level of a control signal [s].

With respect to claim 3, Chang et al. discloses, in Fig. 1, that when the logic level the control signal [s] is a first state (high level), the output signal the power-down controller becomes the output of the (M-1)-th divider, and when the logic level of the control signal is a second state (low level), the output signal of the power-down controller becomes the output of the M-th divider.

With respect to claim 4, Chang et al. discloses, in Fig. 1, that the control signal is a clock enable signal used in the synchronous memory device.

With respect to claim 5, Chang et al. discloses, in Fig. 1, that a pulse width of a high-level state any one of claims output signal of the first divider [x8] is the same as a period of the input signal [clock input of x8] of the first divider, and a pulse width of a low-level state of output signals of the second [x9] to M-th [x11] dividers the same as the period of the input signal of the first divider (*via division by 2 process*).

With respect to claim 7, as best understood, Chang et al. discloses, in Fig. 1, a clock dividing method for a DLL (Delay Lock Loop) circuit synchronous memory device for synchronization an external input clock with an internal input clock, the method comprising a step of selectively outputting [output form x12] an output signal of a (M-1)-th divider [x10] and

an output signal of an M-th divider [X11] among M dividers [x8, x9, x10, x11], connected series, for respectively dividing frequency of the input clock signal into 1/2.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Chang et al. ("A Low-Noise CMOS Prescaler for 900 MHz to 1.9 GHz Wireless Applications", IEEE 1999 Custom Integrated Circuits Conference, pp. 597-600) in view of Tran (U.S. Patent No. 5,162,666).

With respect to claim 6, Chang et al. discloses all of the claimed limitations as expressly recited in claim 1 (*the examiner presumes that claim 6 is dependent on claim 1, see Claim Objection*) except for the power-down controller comprises two transmission gates, and the two transmission gates are selectively turned on/off according to the control signal.

Tran discloses, in Fig. 2, a power-down controller [80] comprises two transmission gates, and the two transmission gates are selectively turned on/off according to a control signal [S1].

To configure the circuit of Chang et al. with a power-down controller as taught by Tran for providing a multiplexing function would have been obvious to one of ordinary skill in the art at the time of the invention since Tran teaches that such configuration would minimize loading on select signal lines (*see Tran, col. 1, lines 57-58*).

***Citation of Relevant Prior Art***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Monk (U.S. Patent No. 6,208,179) discloses a dividing circuit including a plurality of transistor stages.

Prior art Monk (U.S. Patent No. 6,133,796) discloses a programmable dividing circuit including a plurality of N similar transistor stages connected in a divide-by-N sequence.

Prior art Shurboff et al. (U.S. Patent No.) discloses a dual modulus prescaler.

***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LINH MY NGUYEN  
PRIMARY EXAMINER